IN THE CLAIMS:

Please CANCEL claims 2 and 4-7 in accordance with the following:

1. (ORIGINAL) A microprocessor comprising:

a CPU which performs certain arithmetic operations;

an address bus connected to the CPU;

a circuit unit which utilizes an address on the address bus; and

a test circuit which generates a test address for testing the circuit unit.

2. (CANCELLED)

3. (ORIGINAL) The microprocessor as claimed in claim 1, wherein the test circuit comprises:

a control circuit which contains a register storing control values;

an address decoder which receives the control values from the control circuit;

a bit pattern register which generates a bit pattern to produce a test address;

a rotator which makes a change to the bit pattern; and

a bus driver which receives the test address and drives the address bus.

4-7. (CANCELLED)